a Whatis claimed is

~~Patent Claims~~

~~1. Method for standby circuiting of assemblies in 1:N redundancy,~~ comprising

peripheral line assemblies (BG_1...BG_n) that are respectively allocated to one another in pairs and that comprise connections (V_1) to one another via which a mutual monitoring occurs,

at least one standby circuit assembly (BG_E) that takes the place of the down peripheral line assembly in case of a failure of one of the peripheral line assemblies (for example, BG_1), as well as

comprising internal and external interfaces that have an interactive connection to the peripheral line assemblies (BG_1...BG_n) and comprising a higher-ranking means (MPSA) that monitors and controls all devices,

characterized in that

the outage of one of the peripheral line assemblies (for example, BG_1) is determined by the remaining peripheral line assembly (for example, BG_2) allocated paired;

a message (M_E) is subsequently sent from the peripheral line assembly (for example, BG_2) determining the outage to the standby circuit assembly (BG_E), whereupon the latter switches the internal and external interfaces by driving switches (S_1, S_2) and only then activates itself.

2. Method according to claim 1, characterized in that the peripheral line assembly (for example, BG_2) determining the outage additionally sends an outage message (M_A) to the higher-ranking means (MPSA).

3. Method according to claim 1, characterized in that the outage of one of the peripheral line assemblies (for example, BG_1) is additionally recognized by an interfaces [sic] (AMX) belonging to the switching network, where upon this sends a corresponding message (M_{LPS}) to the higher-ranking means (MPSA).